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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.
09/266,237	03/10/99	FARNWORTH	W 97-1433

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MMC1/0618

EXAMINER

ROBERT, R

ART UNIT

PAPER NUMBER

2858

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Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner of Patents and Trademarks

# Office Action Summary

Application No.

09/266,237

Applicant(s)

FARNWORTH ET AL.

Examiner

Russell M Kobert

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

## Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136 (a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

## Status

- 1) ☒ Responsive to communication(s) filed on 30 April 2001.
- 2a) ☐ This action is FINAL. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

## Disposition of Claims

- 4) ☒ Claim(s) 1-48 is/are pending in the application.
- 4a) Of the above claim(s) 3,4,13-16,19-24,28-30 and 33-48 is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1,2,5-12,17,18,25-27,31 and 32 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claims \_\_\_\_\_ are subject to restriction and/or election requirement.

## Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are objected to by the Examiner.
- 11) ☐ The proposed drawing correction filed on \_\_\_\_\_ is: a) ☐ approved b) ☐ disapproved.
- 12) ☐ The oath or declaration is objected to by the Examiner.

## Priority under 35 U.S.C. § 119

- 13) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

## Attachment(s)

- 15) ☒ Notice of References Cited (PTO-892)
- 16) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 17) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 2 and 5.
- 18) ☐ Interview Summary (PTO-413) Paper No(s). \_\_\_\_\_.
- 19) ☐ Notice of Informal Patent Application (PTO-152)
- 20) ☐ Other: \_\_\_\_\_.

1. Applicant's election of Invention I, species 2, claims 1, 2, 5-12, 17, 18, 25-27 and 31-32 in Paper No. 6 is acknowledged. Because applicant did not distinctly and specifically point out the supposed errors in the restriction requirement, the election has been treated as an election without traverse (MPEP § 818.03(a)).
2. Claims 3, 4, 13-16, 19-24, 28-30 and 33-48 are withdrawn from further consideration pursuant to 37 CFR 1.142(b) as being drawn to a nonelected Invention and/or species, there being no allowable generic or linking claim. Election was made **without** traverse in Paper No. 6.
3. In the Brief Description of the Drawings, page 6, line 29, reference to "Figure 1B" is not shown in the drawings. Perhaps reference to Figure 2B should have been intended. Correction is required.
4. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and, *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).  
A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).  
Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

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5. Claims 1, 2, 5-12, 17, 18, 25-27 and 31-32 are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1-24 of U.S. Patent No. 5,962,921 ('921 patent). Although the conflicting claims are not identical, they are not patentably distinct from each other because the claims of the present application are broader than those of the '921 patent.

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

(e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

7. Claims 1, 2, 5-12, 17, 18, 25-27 and 31-32 are rejected under 35 U.S.C. 102(e) as being anticipated by Fjelstad et al (6086386).

Fjelstad et al anticipates (Figure 3) an interconnect for testing a semiconductor component comprising:

a substrate (10);

a contact (22) on the substrate comprising a recess (27) in the substrate, and a plurality of leads (28) cantilevered over the recess (col 6, ln 38-47) configured to move within the recess to electrically engage a bumped contact on the component, each lead comprising at least one projection (bumps or asperities; see col 9, ln 60 – col 10, ln 1)

for penetrating the bumped contact (46), and a non-bonding outer layer (col 10, ln 33-44) for preventing bonding of the lead to the bumped contact;

as recited in claim 1.

Fjelstad et al anticipates (Figure 3) an interconnect for testing a semiconductor component comprising:

a substrate (10);

a recess (27) in the substrate;

a plurality of leads (28) on the substrate cantilevered over the recess (col 6, ln 38-47) and configured to move within the recess to electrically engage a bumped contact (46) on the component, each lead having a cantilever length, a width, a thickness and a modulus of elasticity selected to provide a desired spring constant (col 10, ln 1-21); and

a conductive connecting segment (21a; see Figure 2B) proximate to the recess electrically connecting the leads to one another;

as recited in claim 6.

Fjelstad et al anticipates (Figure 5) an interconnect for testing a semiconductor component comprising:

a substrate (24);

a recess (27) in the substrate;

a plurality of leads (71) on the substrate cantilevered over the recess and configured to move within the recess to electrically engage a bumped contact (46) on

the component, the leads having a curved shape (shown but not labeled) which substantially matches a topography of the bumped contact;

as recited in claim 12.

Fjelstad et al anticipates (Figures 3 and 6) a system for testing a semiconductor component comprising:

a carrier (80) for retaining the semiconductor component (45);

an interconnect (10) on the carrier comprising a substrate (24), a recess (27) in the substrate, and a plurality of leads (71) cantilevered over the recess configured to move within the recess to electrically engage a bumped contact (46) on the component, each lead comprising at least one projection for penetrating the bumped contact (bumps or asperities; see col 9, ln 60 – col 10, ln 1), and a non-bonding outer layer for preventing bonding of the lead to the bumped contact (col 10, ln 33-44); and

test circuitry in electrical communication with the leads for applying test signals to the component (col 6, ln 12-17);

as recited in claim 25.

Fjelstad et al anticipates (Figures 3 and 6) a system for testing a semiconductor component comprising:

a wafer prober (80);

an interconnect (10) mounted to the wafer prober comprising:

a substrate (24);

a recess (27) in the substrate;

a plurality of leads (71) on the substrate cantilevered over the recess and configured to move within the recess to electrically engage a bumped contact (46) on the component, each lead having a cantilever length, a width, a thickness and a modulus of elasticity (col 10, ln 1-21) selected to provide a desired spring constant;

a conductive connecting segment proximate to the recess electrically connecting the leads to one another (21a; see Figure 2B); and

test circuitry (col 6, ln 12-17) in electrical communication with the connecting segment;

as recited in claim 31.

Moreover, the limitations of claims 2, 5, 7-11, 17, 18, 26-27 and 32 are considered inherent in the apparatus of Fjelstad et al or are within the normal range of operating the apparatus of Fjelstad et al.

8. Claims 1, 2, 5-12, 17, 18, 25-27 and 31-32 are rejected under 35 U.S.C. 102(e) as being clearly anticipated by Farnworth et al (5962921; see Figure 7) or Farnworth et al (5756370).

9. Claims 1, 2, 5-12, 17, 18, 25-27 and 31-32 are rejected under 35 U.S.C. 102(b) as being clearly anticipated by Barabi et al (5629837).

10. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

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Lee et al (4686468) and Lim et al (5572140) show an interconnect for testing a semiconductor component having a plurality of leads cantilevered over a recess configured to move within the recess to electrically engage a contact on the semiconductor component.

11. A shortened statutory period for response to this action is set to expire three months from the date of this letter. Failure to respond within the period for response will cause the application to become abandoned. 35 U.S.C. 133

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Russell Kobert whose telephone number is (703) 308-5222.

Any inquiry of a general nature or relating to the status of this application should be directed to the Group receptionist whose telephone number is (703) 308-0956.



Russell M. Kobert  
Patent Examiner  
Group Art Unit 2858  
June 11, 2001



ERNEST KARLSEN  
PRIMARY EXAMINER